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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ART UNIT	**PAPER NUMBER**
3663	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,714	LUK ET AL.	
	Examiner	Art Unit	
	JOHANNES P. MONDT	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-28,36 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-28, 36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 5/6/08 forms the basis for this Office Action. In said Amendment Applicants cancelled claims 21-23 and 29-35 and amended all remaining, pending claims at least through substantial amendments to claims 24, 27 and 28. Said pending claims, i.e., claims 24-28, 36 and 37 are being examined. Comments on "Remarks" filed with said Amendment, are included below under "Response to Arguments".

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 24-28, 36 and 37*** are rejected under 35 U.S.C. 102(b) as being anticipated by Folmsbee (5,386,151).

Folmsbee teaches as prior art (Figure 1A and col. 4, l. 1-65) a method for amplifying signals ("Description of the Preferred Embodiment", col. 1, l. 29-32 and col. 3, l. 57-67), the method comprising:

determining that a voltage on a signal line (signal line from VDD, as arriving at node 125) is to be amplified;

modifying voltage on a control line ϕ' (providing clock input ϕ' under gate of MOS capacitor 130) (col. 4, l. 1-33), wherein the control line is coupled to a

second terminal (source-drain terminal) of a two-terminal semiconductor device (MOS capacitor 130) (Fig. 1A and loc.cit.), the two-terminal device having said second terminal and a first terminal (gate), the first terminal coupled to the signal line (Fig. 1A and loc.cit.) , the second terminal coupled to the control line (see above), wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal is in a first voltage range and to have a lower capacitance when a voltage on the first terminal (gate) is in a second voltage range (inherently so because the MOS capacitor's conductive channel width and conductivity depends thus on gate voltage), wherein said first and second voltage ranges are defined by a threshold voltage (inherently so, for the formation of a conductive channel is characterized by a threshold voltage), and wherein the control line is adapted to be coupled to a control signal (clock signal ϕ') and wherein the signal line is adapted to be coupled to a signal and to be an output VOUT of the circuit (through 140); and

wherein an isolation device (NMOS transistor 110) is intermediate the signal line and the two-terminal semiconductor device, the isolation device having an input, an output and a control terminal (gate of NMOS transistor 110), the input of the isolation device coupled to the signal line (at node 125) and the output of the isolation device coupled to the first terminal 130 (through node 135), wherein the output of the isolation device is adapted to be output of "the" circuit, interpreted to be "output of the amplifier", and wherein the method further comprises the step of applying a control voltage to the control terminal of the

isolation device (a gate voltage is inherently applied to the NMOS transistor's gate when is use), the control voltage being greater than a threshold voltage of the isolation device (as otherwise the isolation device would be a perfect and permanent insulator while no voltage would be communicated).

On claim 25: the limitation is met because the "expected" voltage for a signal coupled to the input of the isolation device is the voltage at node 125, which is added to the voltage on the gate of NMOS transistor 110, i.e., the isolation device (see col. 4, l. 34-40), the gate thereof being in series with said node 125, and the clock input ϕ in a high state adding to the pre-charge voltage at 125 the clock swing of clock input ϕ.

On claim 26: the isolation device comprises a Field Effect Transistor (FET), in particular: a NMOS Field Effect Transistor or NMOSFET (loc.cit.), which is adapted to be turned on when the voltage on the signal line is below a predetermined value (because the source-drain voltage, for any given voltage on either drain or source, in a neighborhood of $-\infty$ for either source or drain, respectively, conducts because of the finite value of the turn-ON threshold of said isolation device, and is adapted to be turned off when voltage on the first terminal of the two-terminal semiconductor device is above a predetermined value, because for any given voltage at node 125 said isolation device is on in a neighborhood of ∞ and is turned off when the voltage at node 135 crosses the turn-OFF threshold (col. 4, l. 34-48)

On claims 27-28: the control terminal of the FET is the gate of the FET (110) and the step of applying a control voltage to the control terminal of the isolation device

comprises the step of applying a voltage above and below a threshold voltage to the gate of the FET through clock-input control ϕ. (col. 4, l. 41-43).

On claim 36: the step of generating the control voltage further comprises the step of generating the control voltage by using at least a reference voltage (Ground, to which substrate of MOS capacitor 120 is connected) and the control voltage (through clock input ϕ) (Figure 1A for grounding, as well as col. 4, l. 1-20).

On claim 37: the step of generating the reference voltage comprises the step of using a ground voltage (loc.cit.).

Response to Arguments

1. Applicant's arguments filed 5/6/08 have been fully considered but they are not in all respects persuasive, although the amendments successfully overcome the rejection under 35 USC 112, second paragraph and the objection for minor informalities.

With regard to Applicants' argument in traverse of the rejection of independent claim 24, Applicants' basis for said traverse appears (a) the definition of the IEEE Standard Dictionary of Electrical and Electronic Terms *for example* (sic), "carrying binary true / false logic values", and (b) that a MOS capacitor is a three-terminal device despite the connection of source to drain terminal. See pages 4-5 of "Remarks", especially lines 4-11 on page 5.

Argument (a) is not persuasive, because no example can possibly be a definition, while the very variability of the VDD arriving at node 125 in Folmsbee implies information to which the device of his method responds. Moreover, even arguendo, the

variable voltage VDD not only can be used, and actually is used, in the method employing the device by Folmsbee, to convey information on control, because the voltage source VDD is a modified signal carrying information upon arrival at node 125.

Argument (b) is not persuasive, because even by admission in the Specification (see Figures 2 and discussion, see n-type "gated diode" 100 with source diffusion and drain diffusion regions 210 and 245, respectively, in addition of course to the gate 215) a gated diode is a two-terminal device while having source, gate and drain, with source and drain short-circuited. It is further noted that this terminology, far from repugnant, also is standard in the field of MOS capacitors and MOSFETs.

In light of the above considerations and examination of the newly amended claim language, the amended claims are again rejected under 35 USC 102(b) as anticipated by Folmsbee as previously cited.

Conclusion

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES P. MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Johannes P Mondt/
Primary Examiner, Art Unit 3663